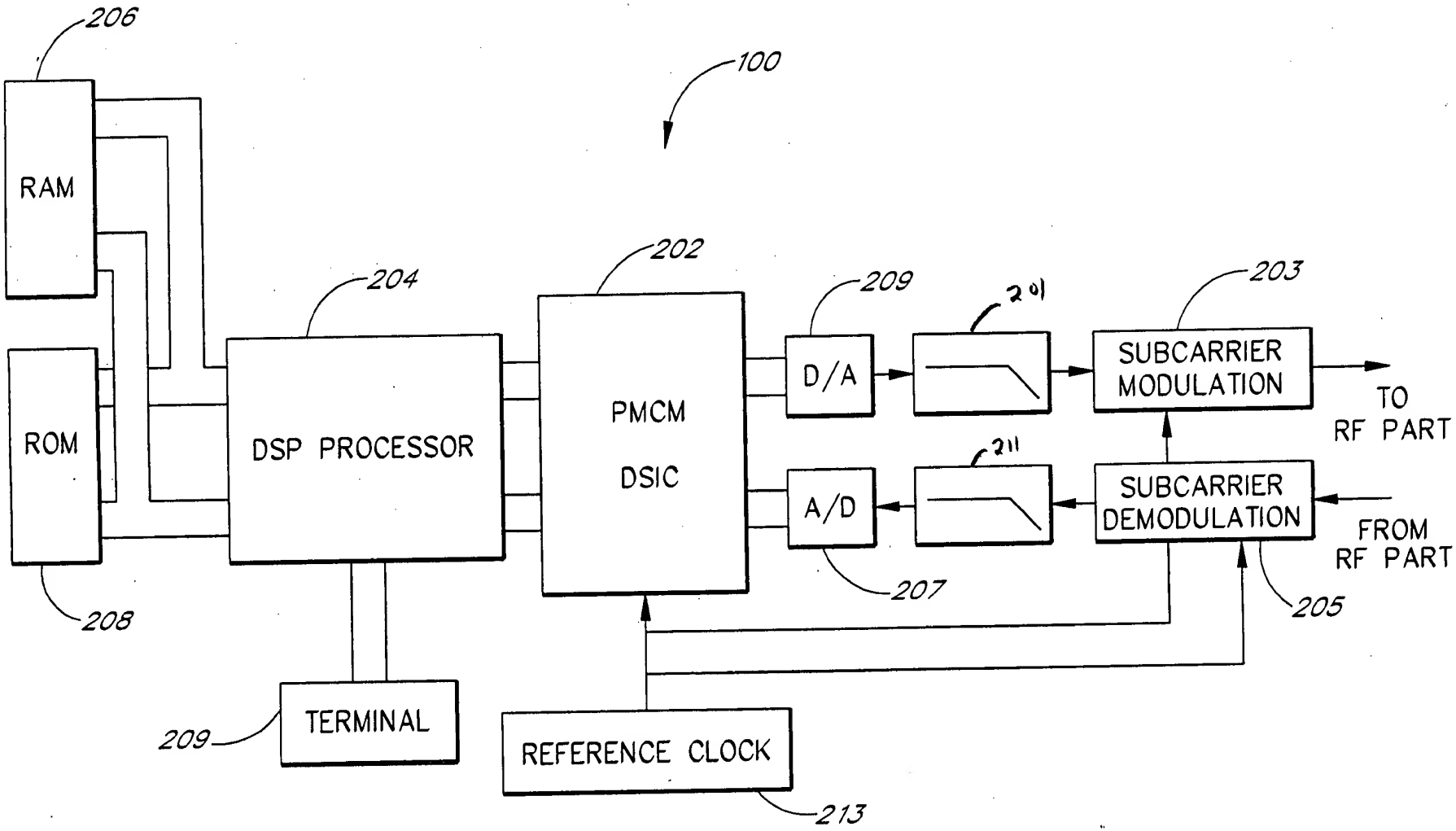

206
100
RAM
ROM
208
204
DSP PROCESSOR
202
PMCM
DSIC
209
D/A
201
203
SUBCARRIER MODULATION
TO RF PART
211
A/D
207
SUBCARRIER DEMODULATION
FROM RF PART
205
209
TERMINAL
REFERENCE CLOCK
213

FIG. 1

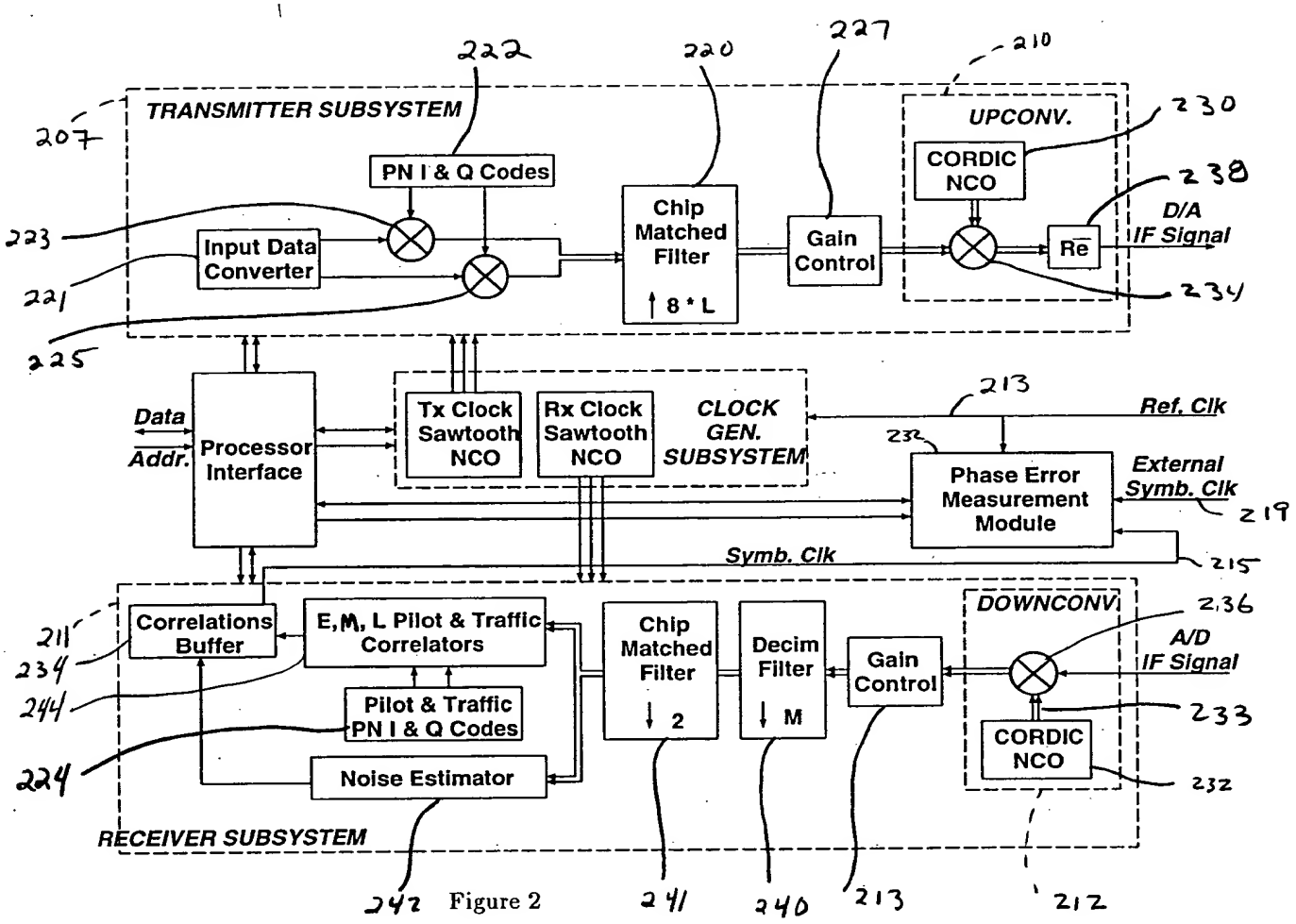


Figure 2

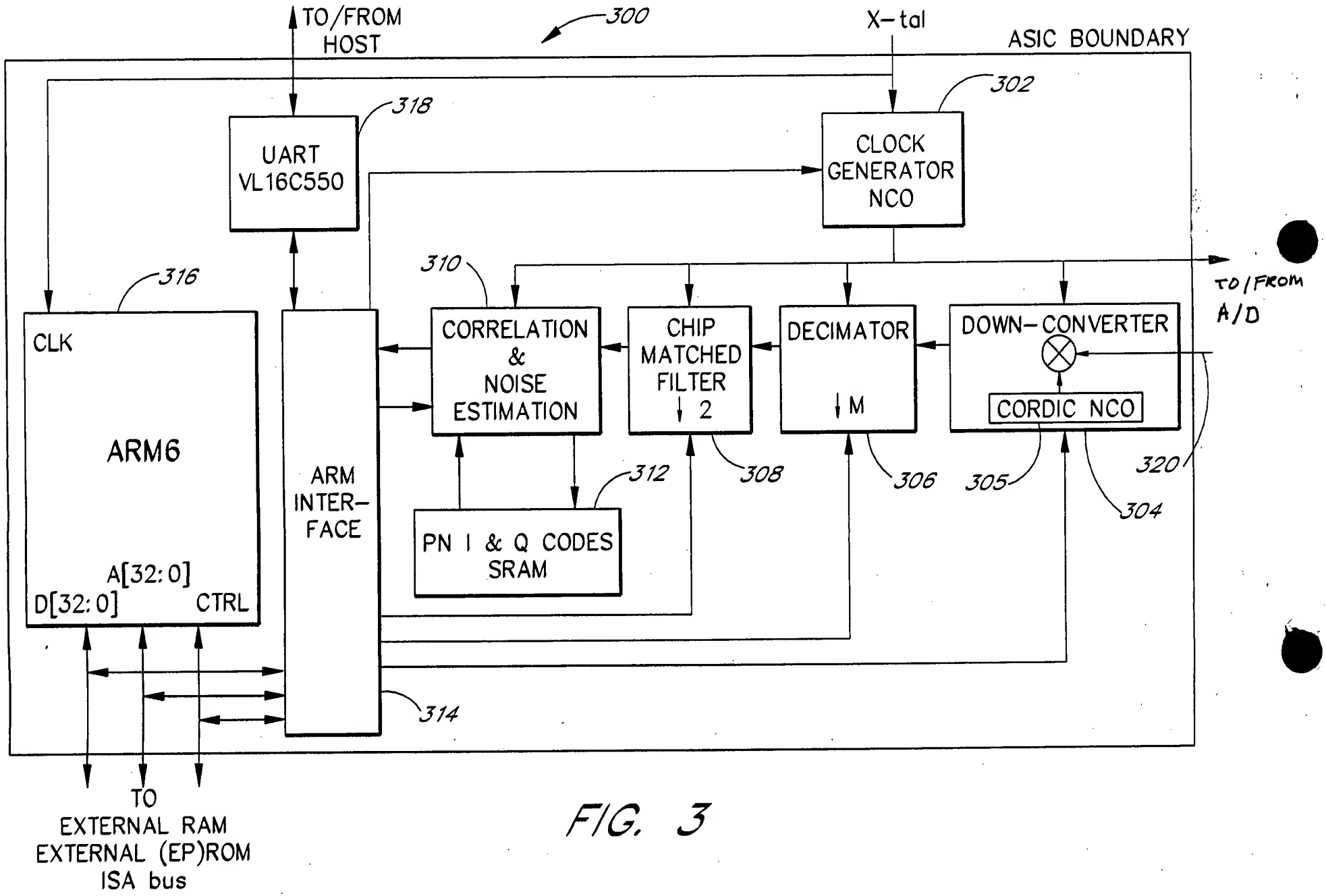

TO/FROM HOST
300
X-tal
ASIC BOUNDARY
318
UART VL16C550
302
CLOCK GENERATOR NCO
316
310
TO/FROM A/D
CLK
ARM6
A[32:0]
D[32:0]
CTRL
ARM INTER-FACE
CORRELATION & NOISE ESTIMATION
CHIP MATCHED FILTER ↓ 2
DECIMATOR ↓ M
DOWN-CONVERTER
CORDIC NCO
312
308
306
305
320
304
PN I & Q CODES SRAM
314
TO EXTERNAL RAM EXTERNAL (EP)ROM ISA bus

FIG. 3

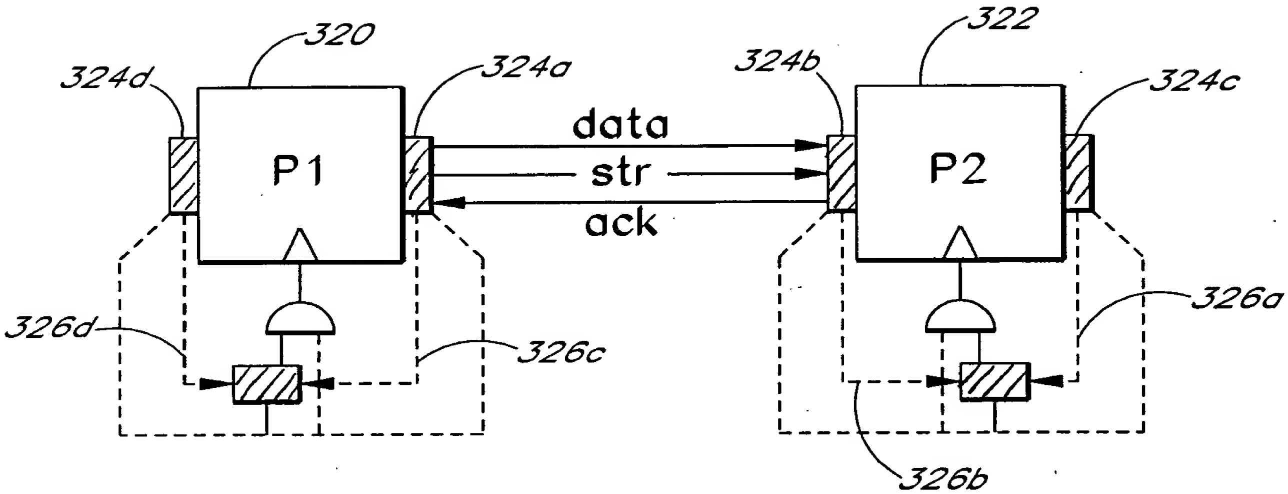


FIG. 4

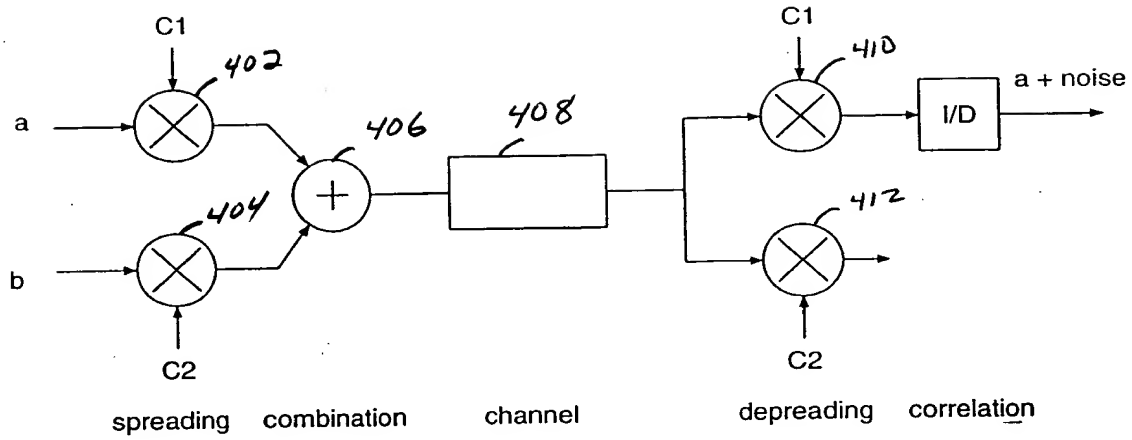


Figure 5:

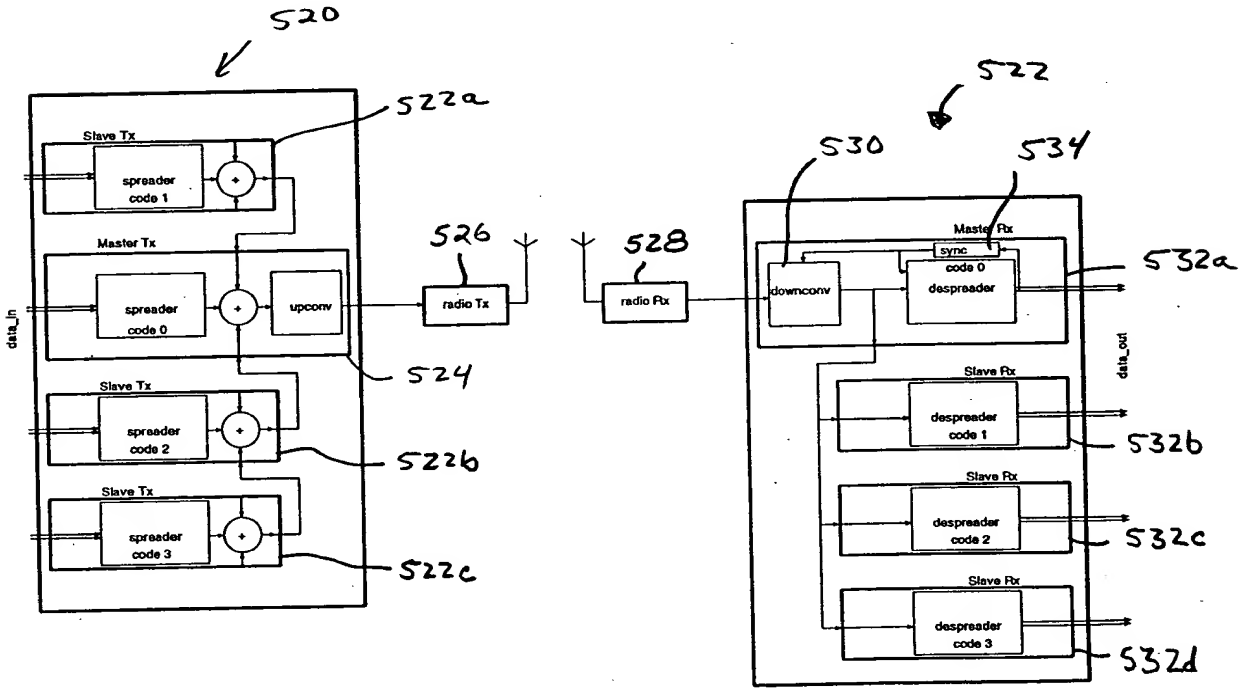


Figure 6

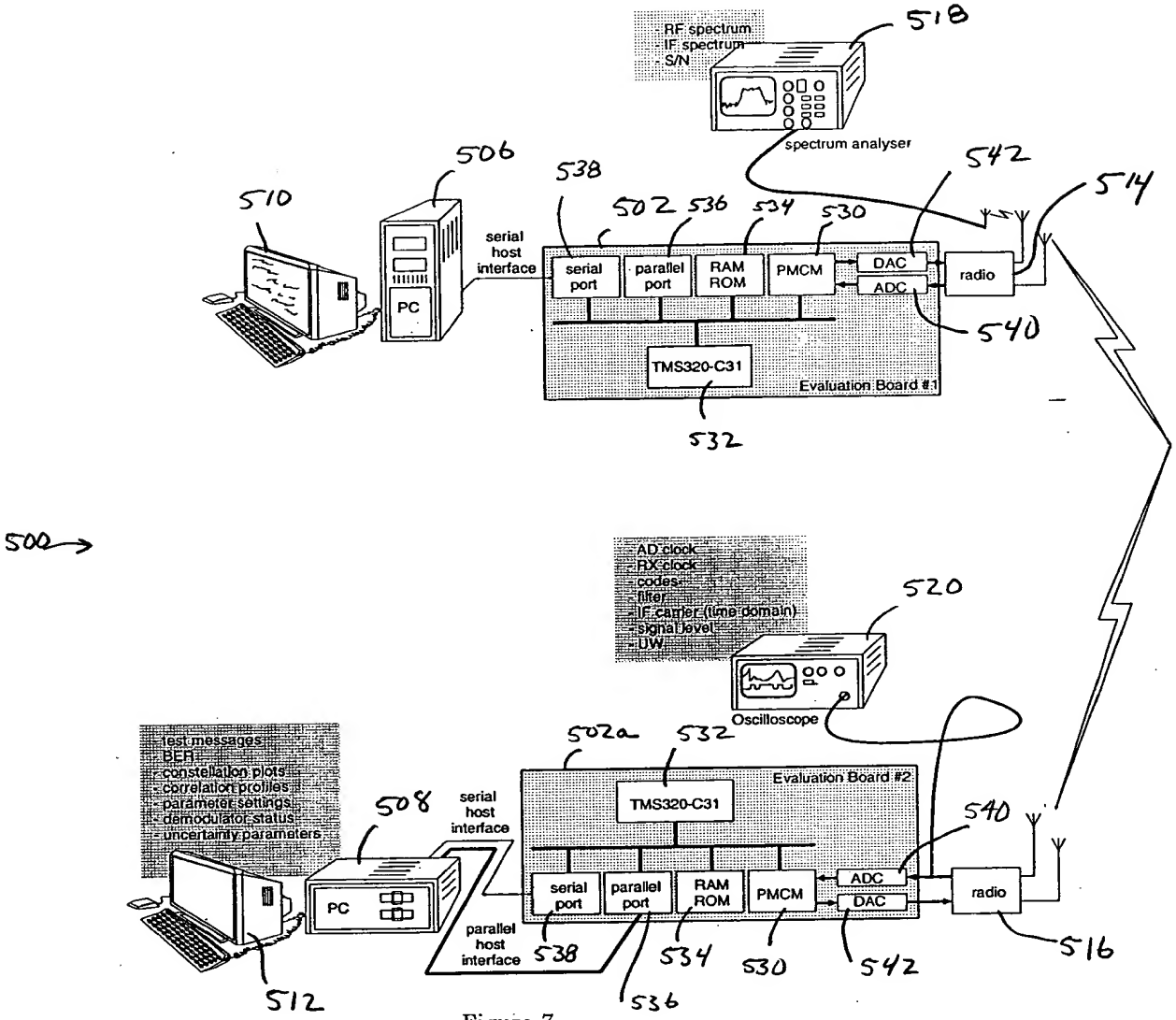

RF spectrum
IF spectrum
S/N
518
spectrum analyser
506
538
542
514
510
502
536
534
530
serial host interface
serial port
parallel port
RAM ROM
PMCM
DAC
ADC
radio
PC
540
TMS320-C31
Evaluation Board #1
532
500
AD clock
RX clock
codes
filter
IF carrier (time domain)
signal level
UW
520
Oscilloscope
test messages
BER
constellation plots
correlation profiles
parameter settings
demodulator status
uncertainty parameters
502a
532
Evaluation Board #2
TMS320-C31
508
serial host interface
serial port
parallel port
RAM ROM
PMCM
ADC
DAC
radio
540
parallel host interface
538
534
530
542
516
512
536

Figure 7

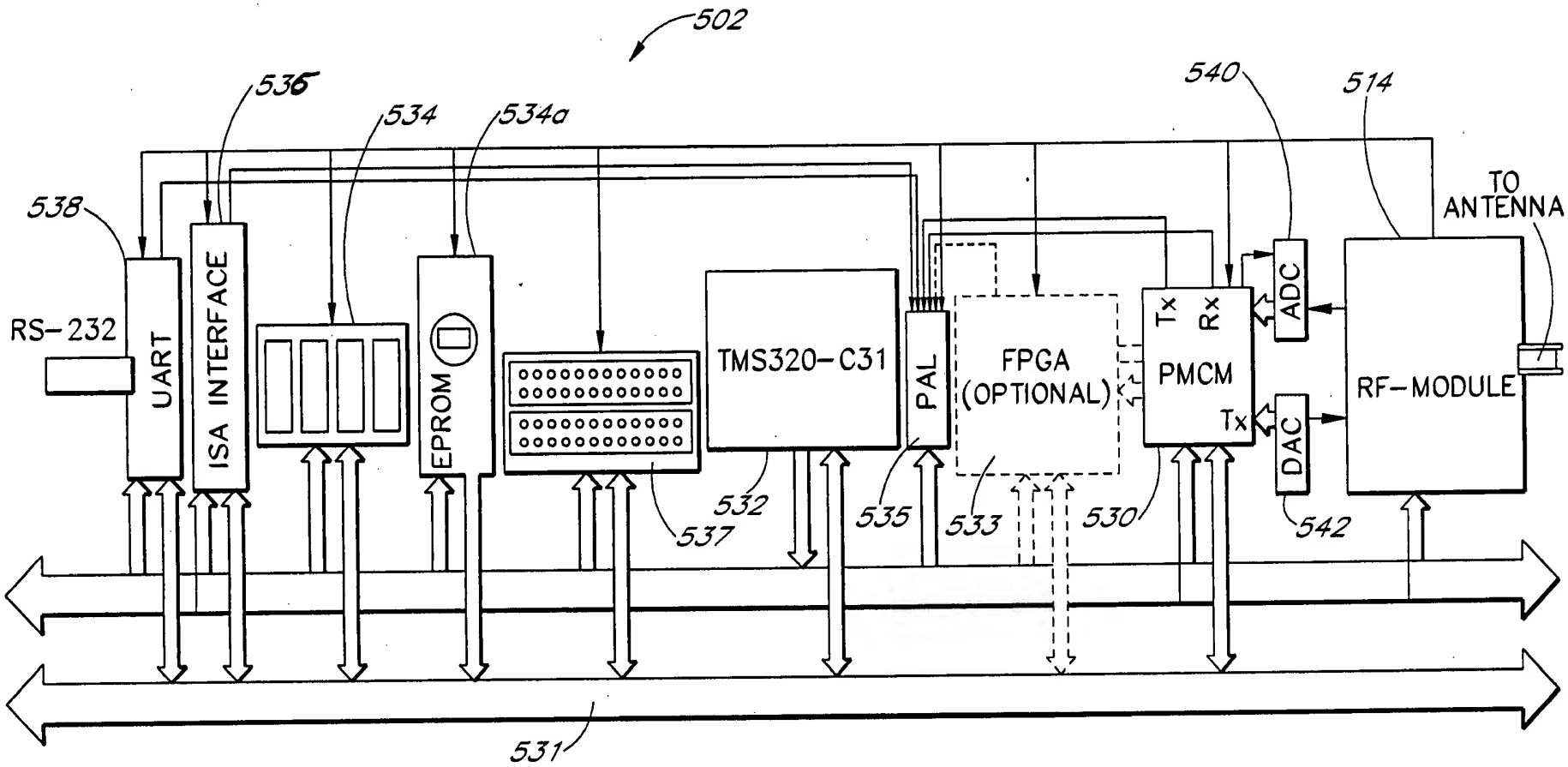

502
536
534
534a
540
514
538
TO ANTENNA
RS-232
UART
ISA INTERFACE
EPROM
TMS320-C31
PAL
FPGA (OPTIONAL)
Tx
Rx
PMCM
Tx
ADC
DAC
RF-MODULE
532
537
535
533
530
542
531

FIG. 8

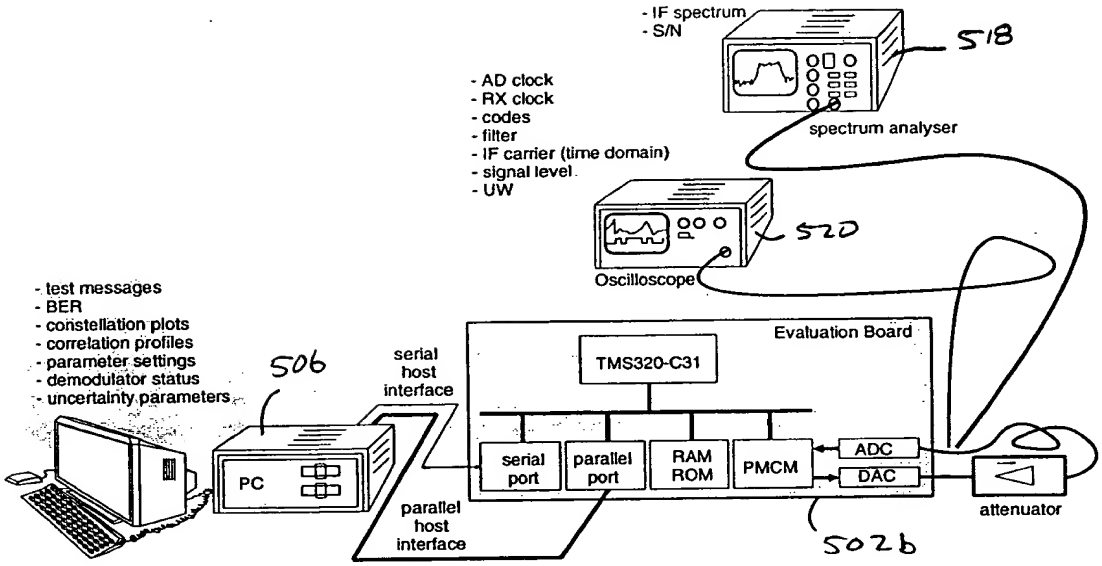


Figure 9:

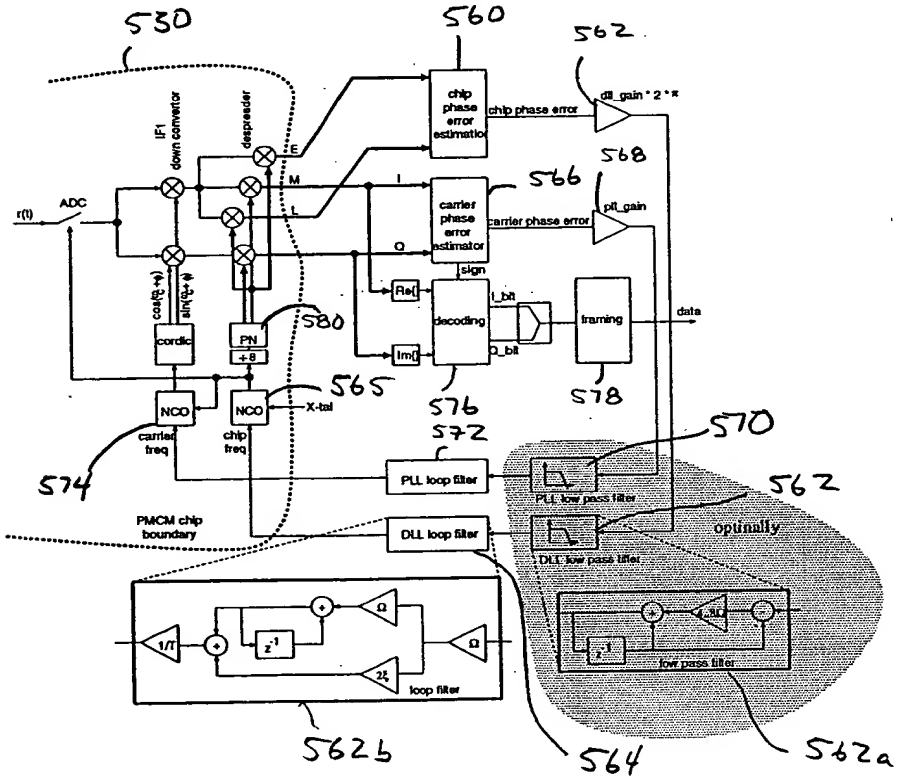


Figure 10

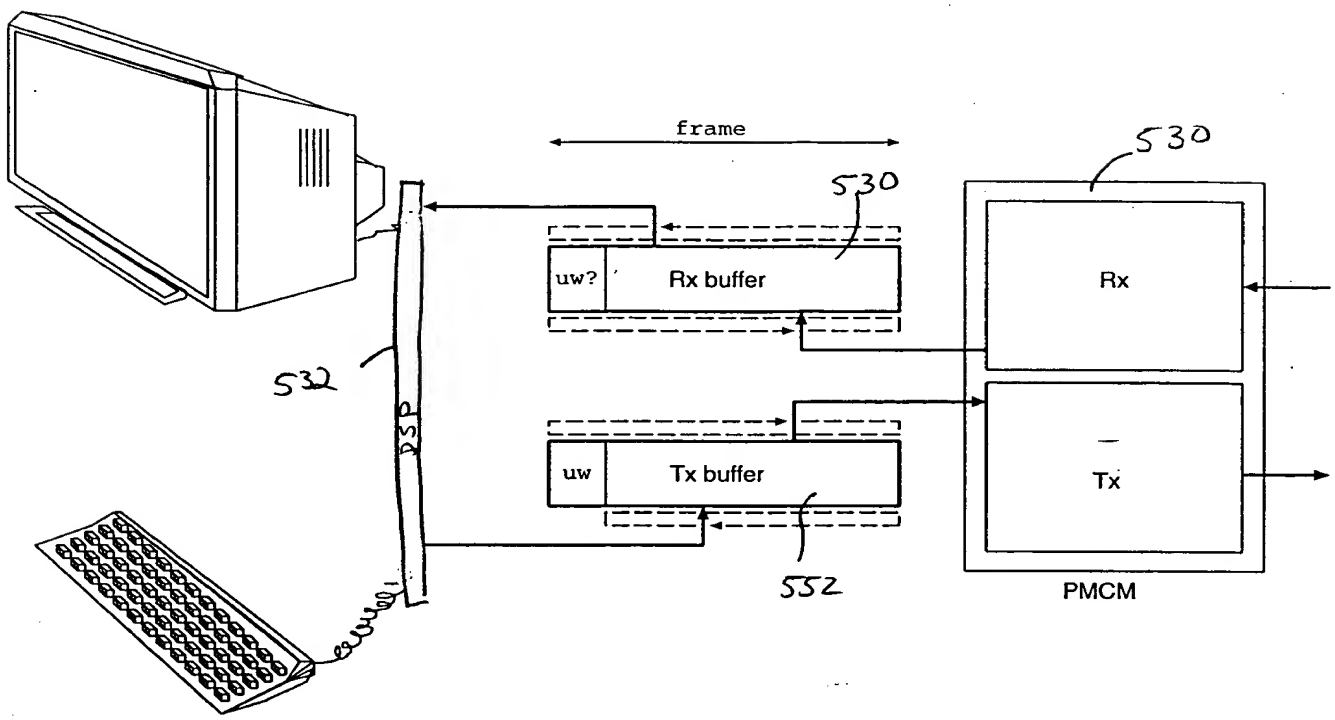


Figure 11

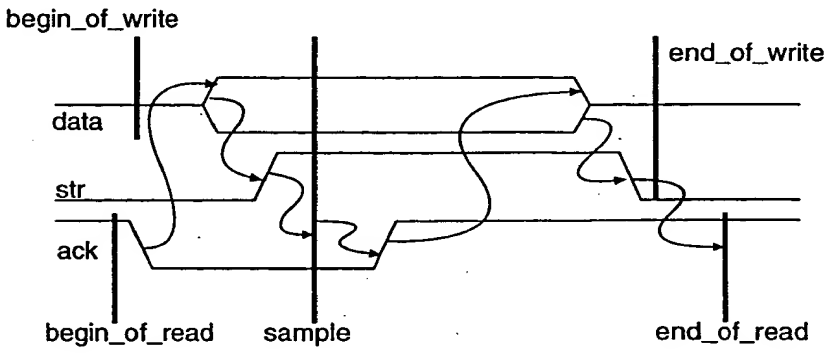


Figure 12

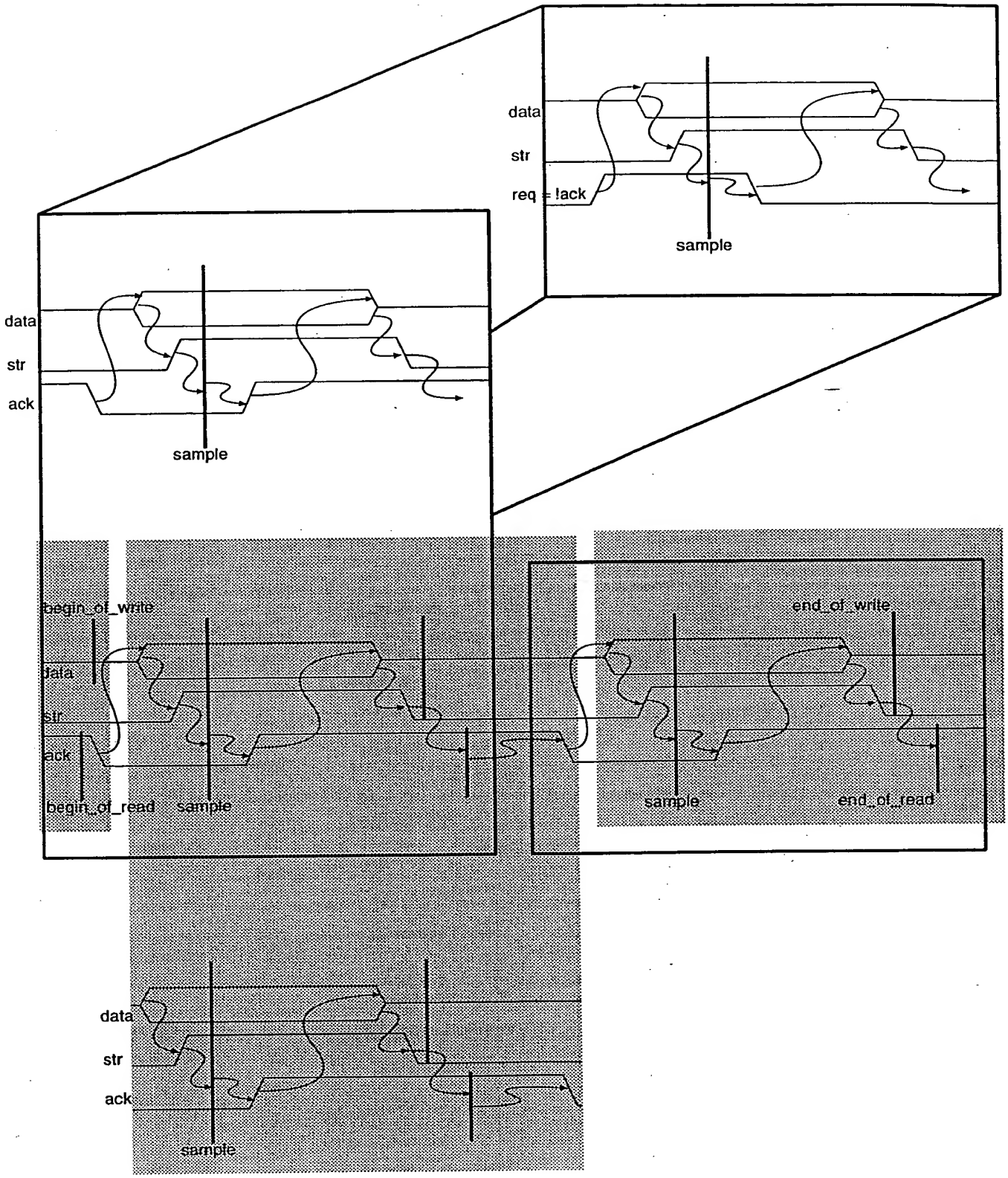

data
str
req = !ack
sample
data
str
ack
sample
begin_of_write
data
str
ack
begin_of_read
sample
end_of_write
sample
end_of_read
data
str
ack
sample

Figure 13

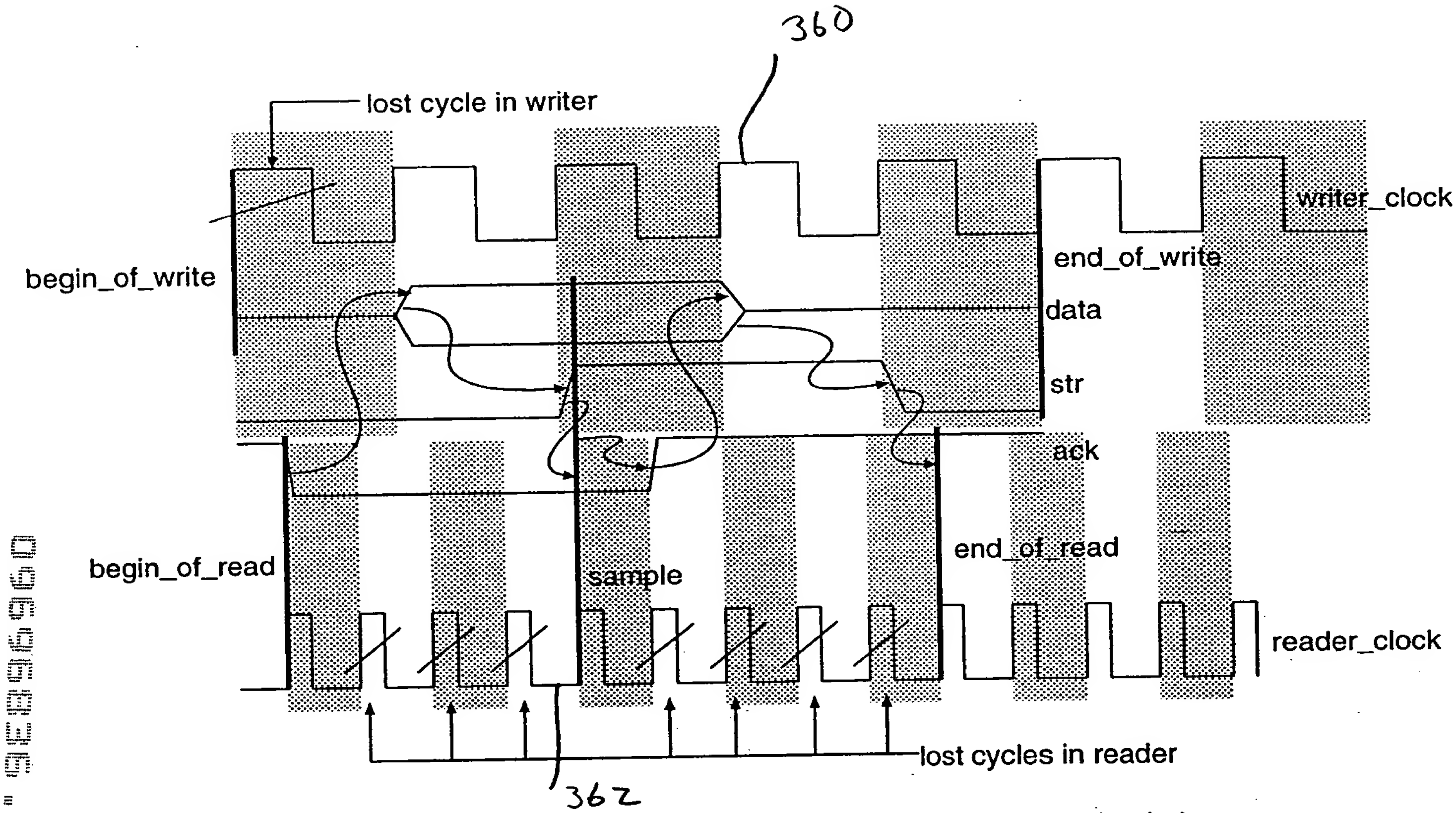
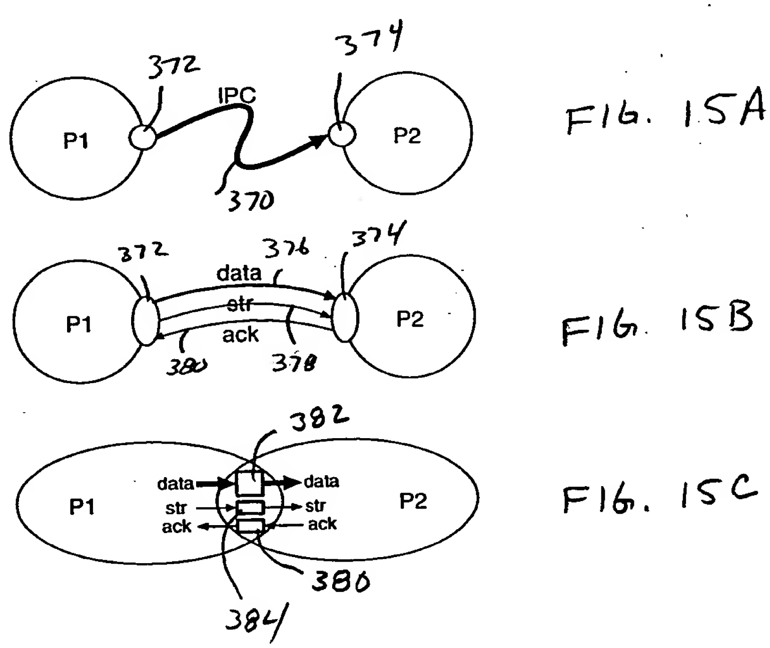


Figure 14.



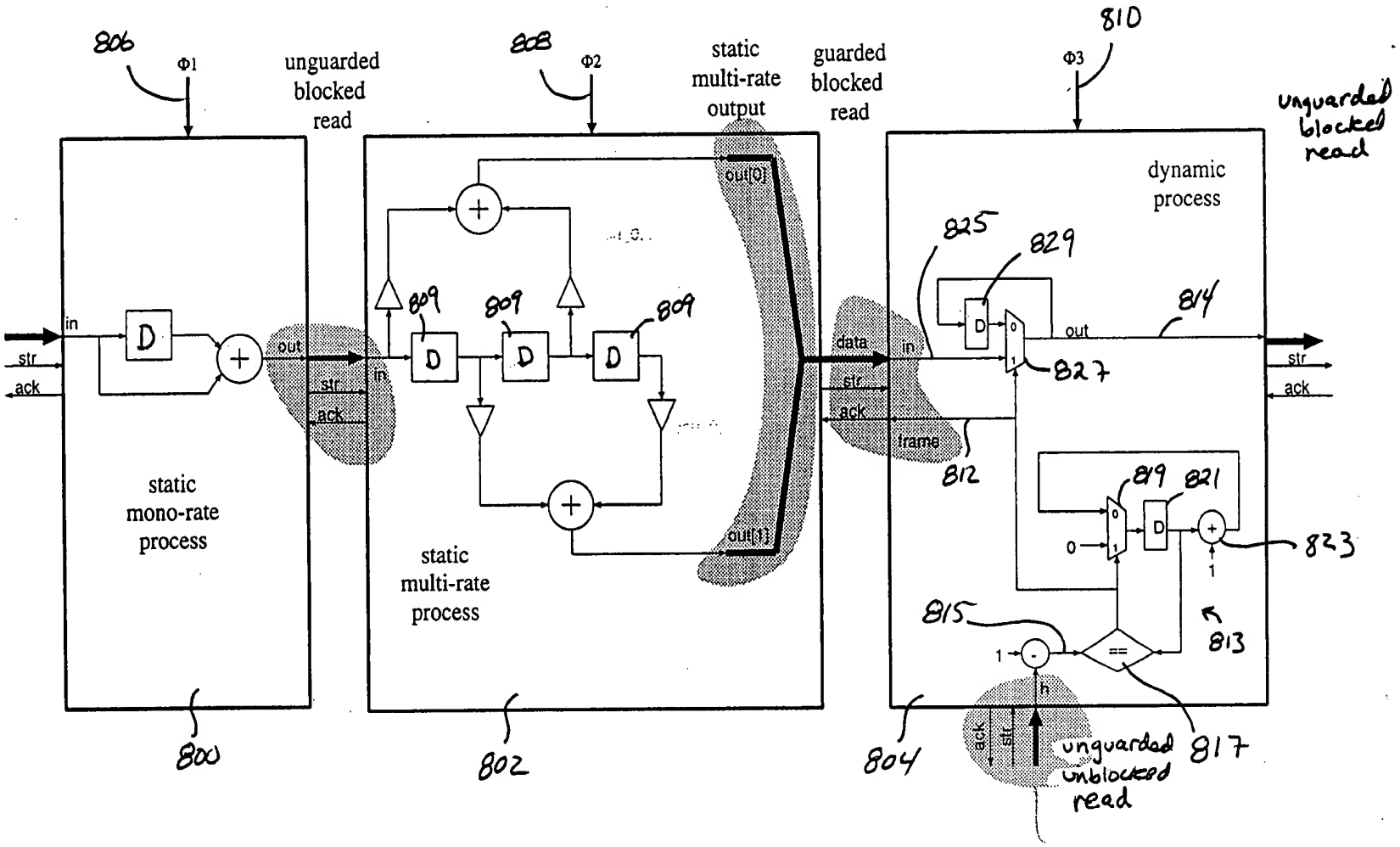

806
Φ1
unguarded blocked read
808
Φ2
static multi-rate output
guarded blocked read
810
Φ3
unguarded blocked read
dynamic process
in
str
ack
D
out
static mono-rate process
800
809
out[0]
out[1]
static multi-rate process
802
data
frame
825
829
827
814
812
819
821
823
815
813
817
804
unguarded unblocked read

Figure 16

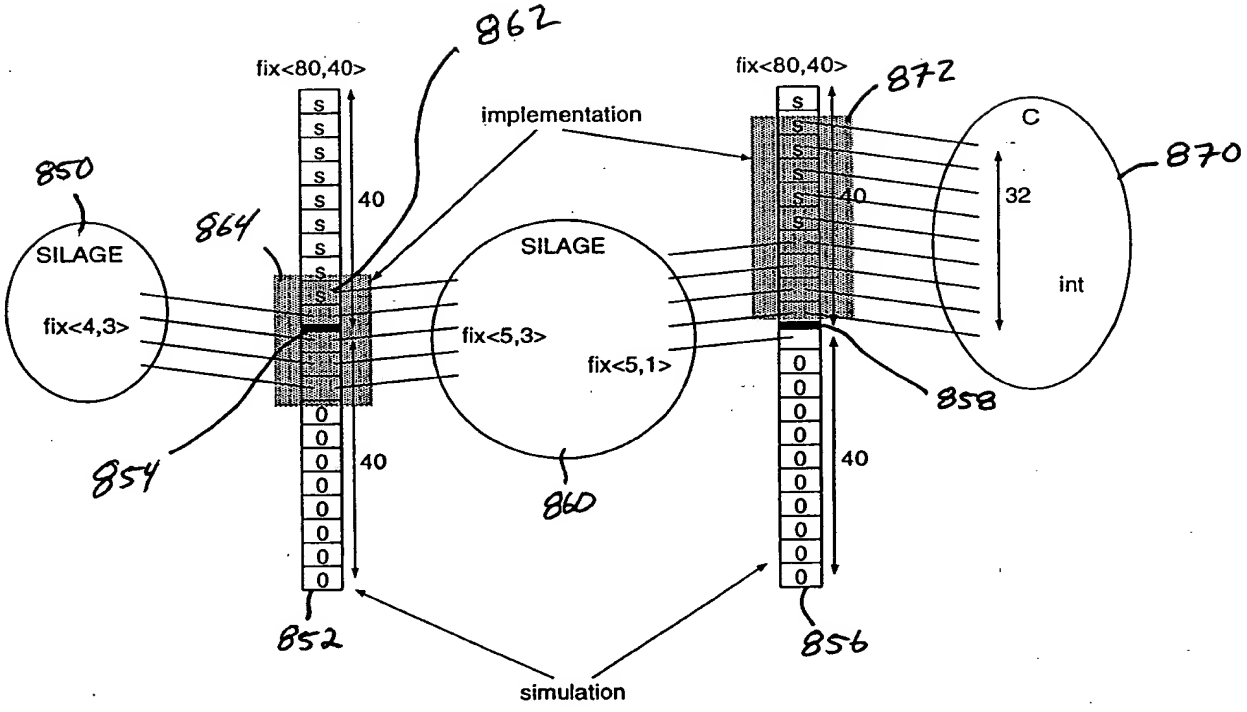

862
fix<80,40>
implementation
fix<80,40>
872
C
870
850
SILAGE
40
32
int
864
SILAGE
fix<4,3>
fix<5,3>
fix<5,1>
858
854
40
40
860
852
856
simulation

Figure 17: C

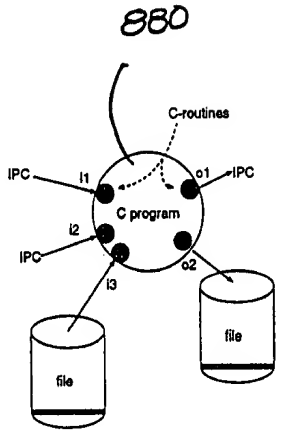


FIG. 18A

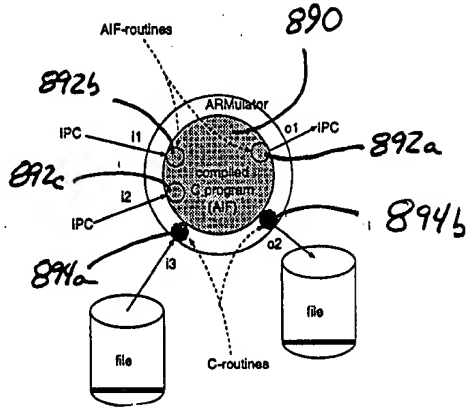


FIG. 18B

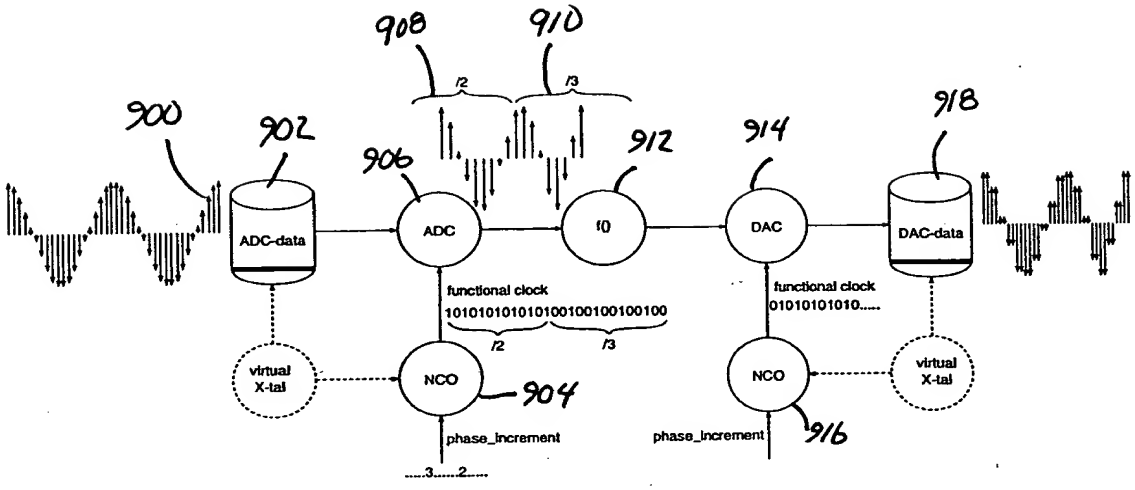


Figure 19

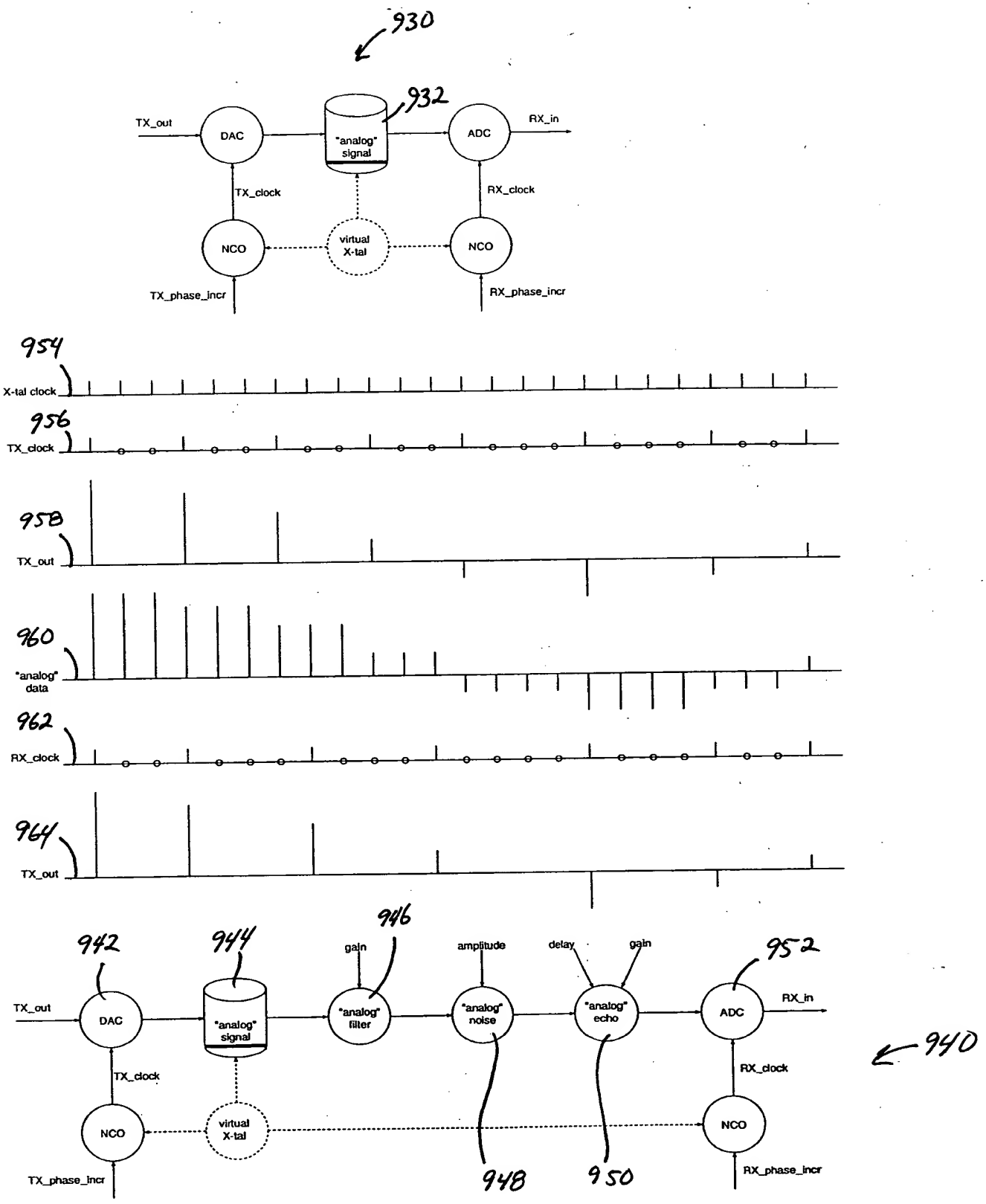

930
932
TX_out
DAC
"analog" signal
ADC
RX_in
TX_clock
RX_clock
NCO
virtual X-tal
NCO
TX_phase_incr
RX_phase_incr
954
X-tal clock
956
TX_clock
958
TX_out
960
"analog" data
962
RX_clock
964
TX_out
942
944
946
gain
amplitude
delay
gain
952
TX_out
DAC
"analog" signal
"analog" filter
"analog" noise
"analog" echo
ADC
RX_in
940
TX_clock
RX_clock
NCO
virtual X-tal
NCO
TX_phase_incr
948
950
RX_phase_incr

Figure 20:

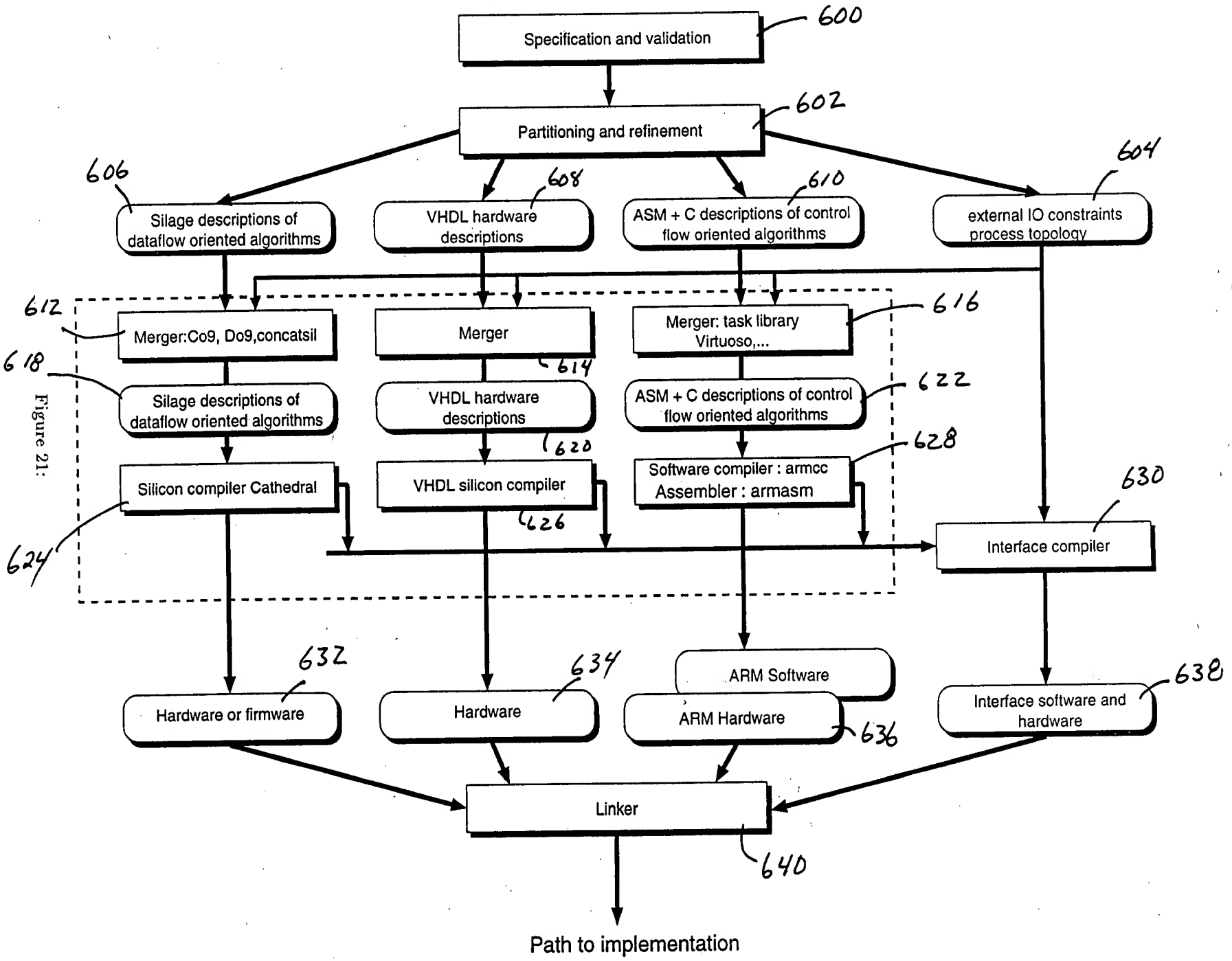

Specification and validation
600
Partitioning and refinement
602
606
Silage descriptions of dataflow oriented algorithms
608
VHDL hardware descriptions
610
ASM + C descriptions of control flow oriented algorithms
604
external IO constraints process topology
612
Merger:Co9, Do9,concatsil
Merger
614
Merger: task library Virtuoso,...
616
618
Silage descriptions of dataflow oriented algorithms
VHDL hardware descriptions
620
ASM + C descriptions of control flow oriented algorithms
622
Silicon compiler Cathedral
624
VHDL silicon compiler
626
Software compiler : armcc
Assembler : armasm
628
630
Interface compiler
632
Hardware or firmware
634
Hardware
ARM Software
ARM Hardware
636
Interface software and hardware
638
Linker
640
Path to implementation

Figure 21:

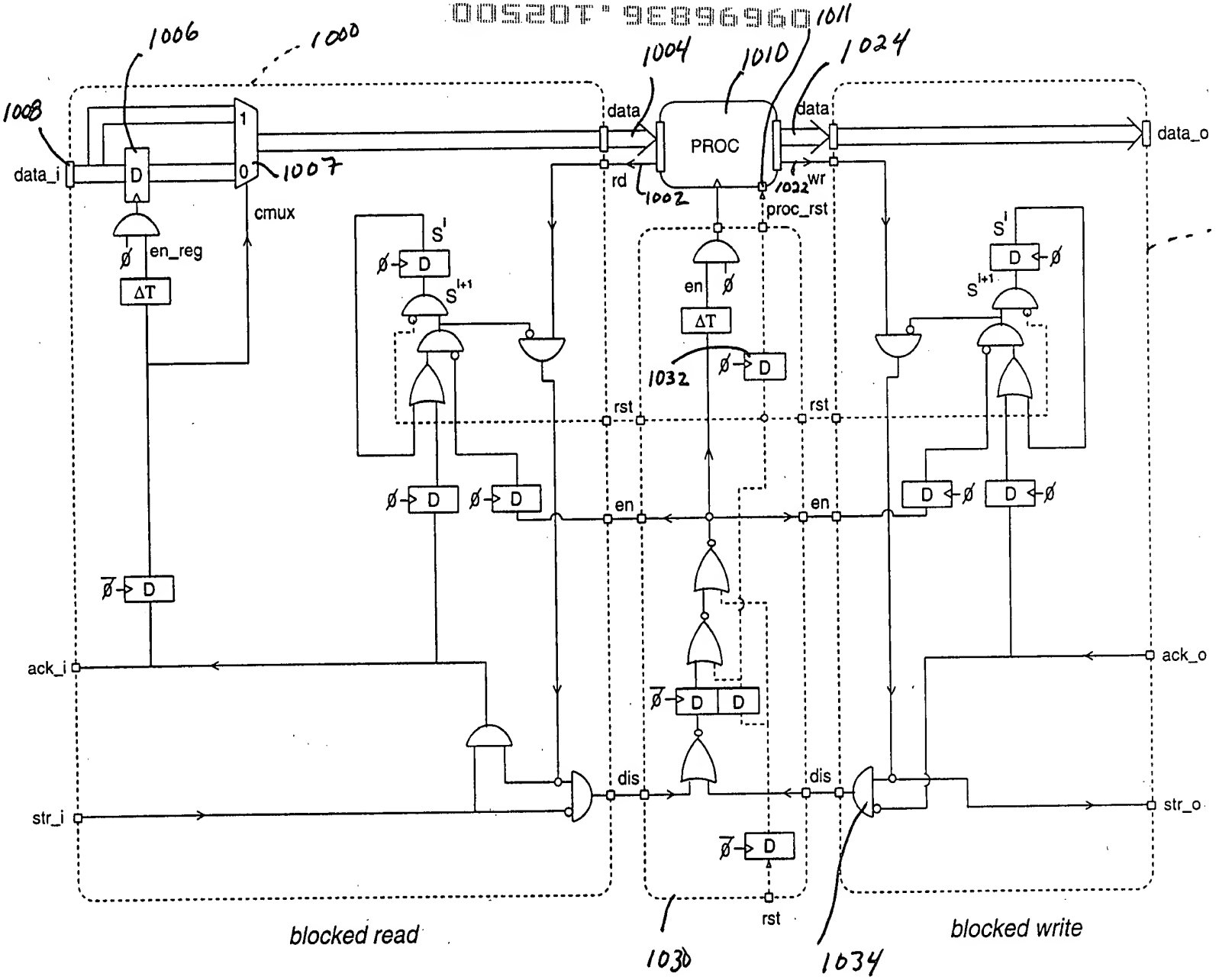


Figure 22.

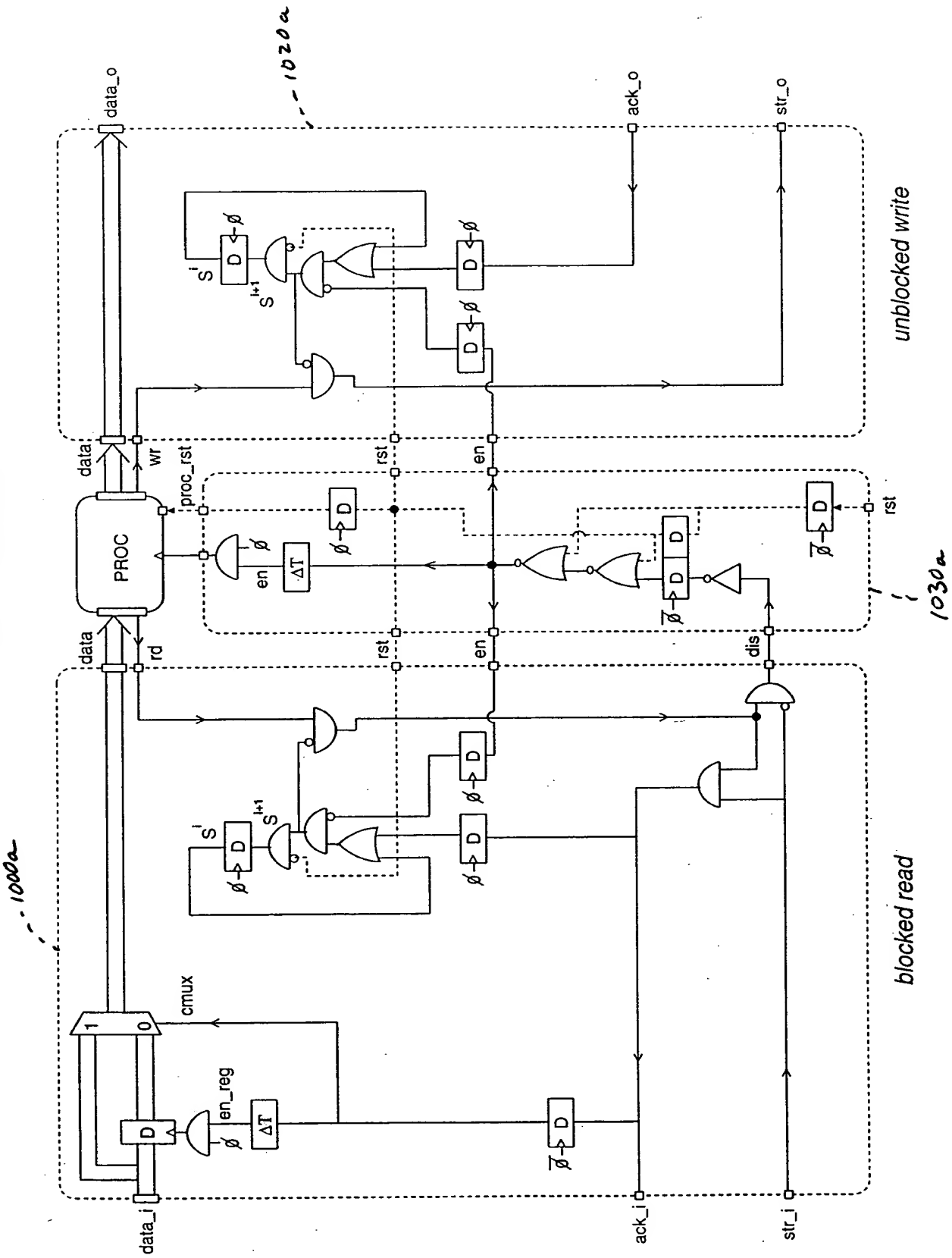

1020a
data_o
ack_o
str_o
unblocked write
data
wr
proc_rst
rst
en
PROC
rd
dis
1030a
blocked read
cmux
en_reg
ΔT
data_i
ack_i
str_i
1000a

Figure 23

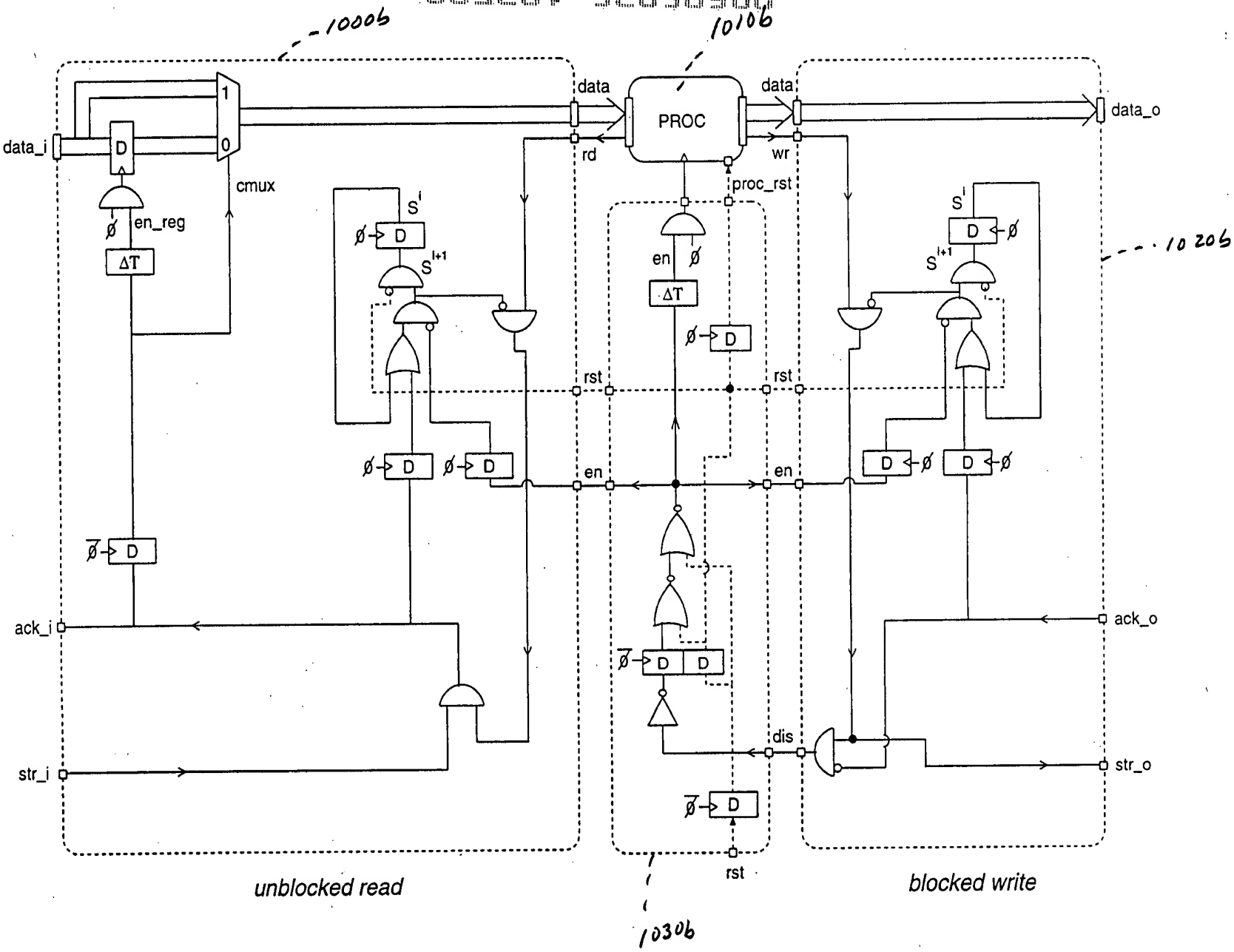


Figure 24

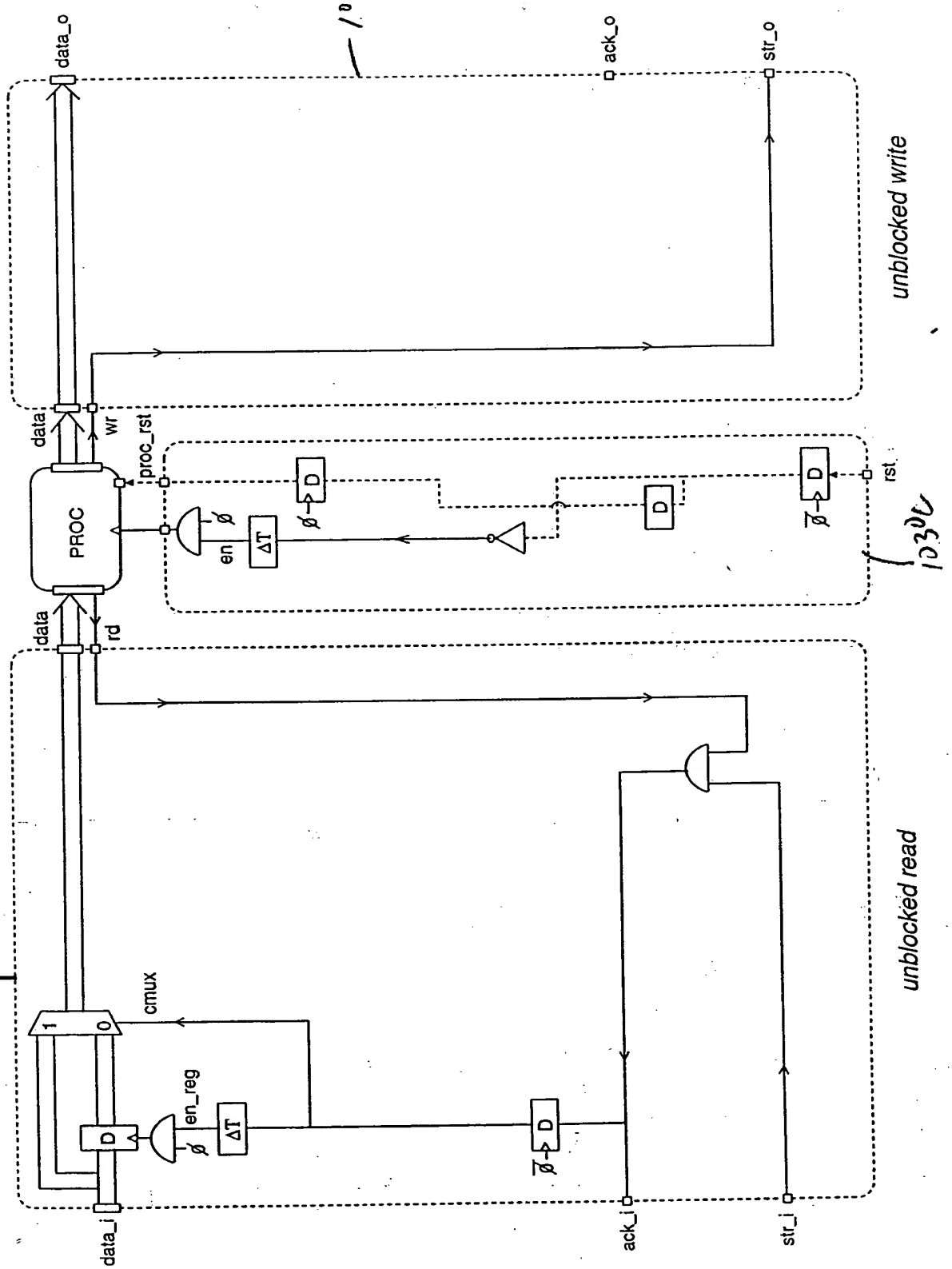

data_o
ack_o
str_o
unblocked write
data
wr
proc_rst
PROC
rst
en
ΔT
D
data
rd
unblocked read
cmux
1
0
en_reg
data_i
ack_i
str_i

Figure 25:

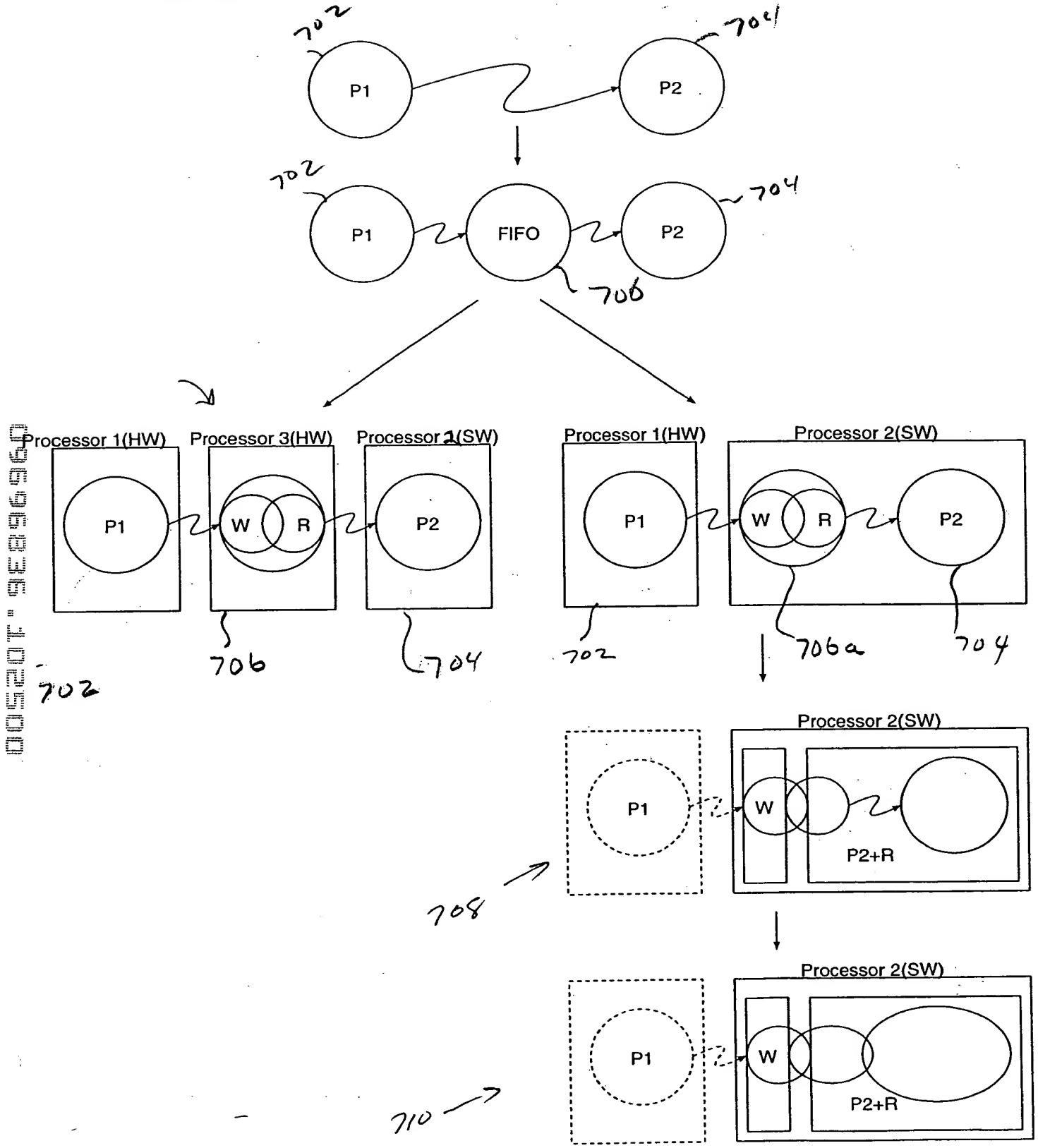
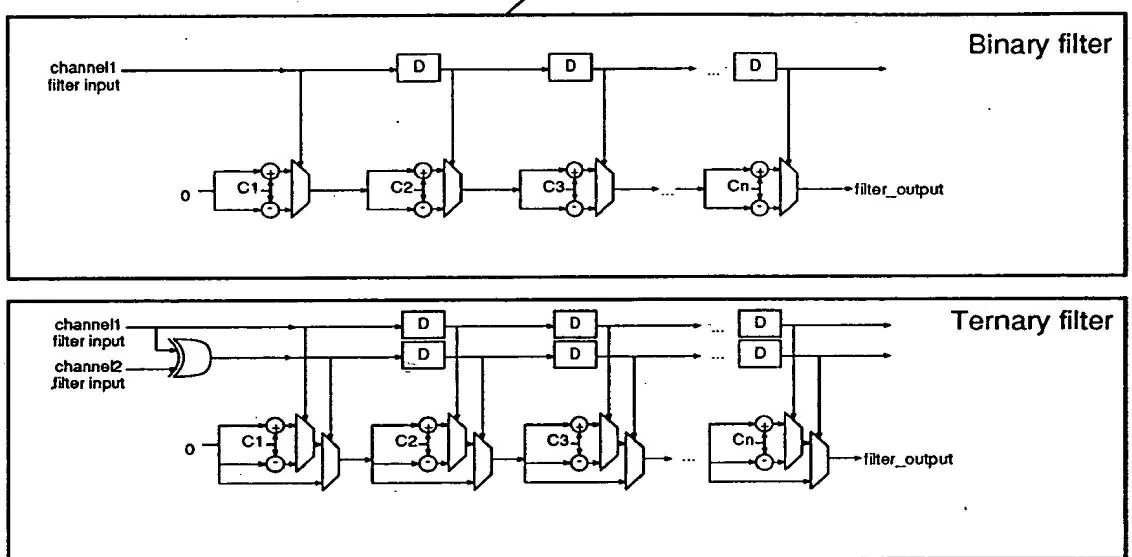


Figure 26: Refinement of a FIFO channel.

330



332

Figure 27

09658836 . 102500